

The diagram illustrates a system architecture divided into two main sections: **HOST SIDE** and **PANEL SIDE**, separated by a dashed line.

**HOST SIDE:**

- A **SYSTEM BUS** (13) connects to a **GRAPHICS CHIP** (11).
- The **GRAPHICS CHIP** (11) is connected to **GRAPHICS MEMORY** (12) via a bus (14).
- The **GRAPHICS CHIP** (11) also includes an internal component (20).
- The **GRAPHICS CHIP** (11) is connected to a **DIGITAL I/F LINE** (49) via a component (15).

**PANEL SIDE:**

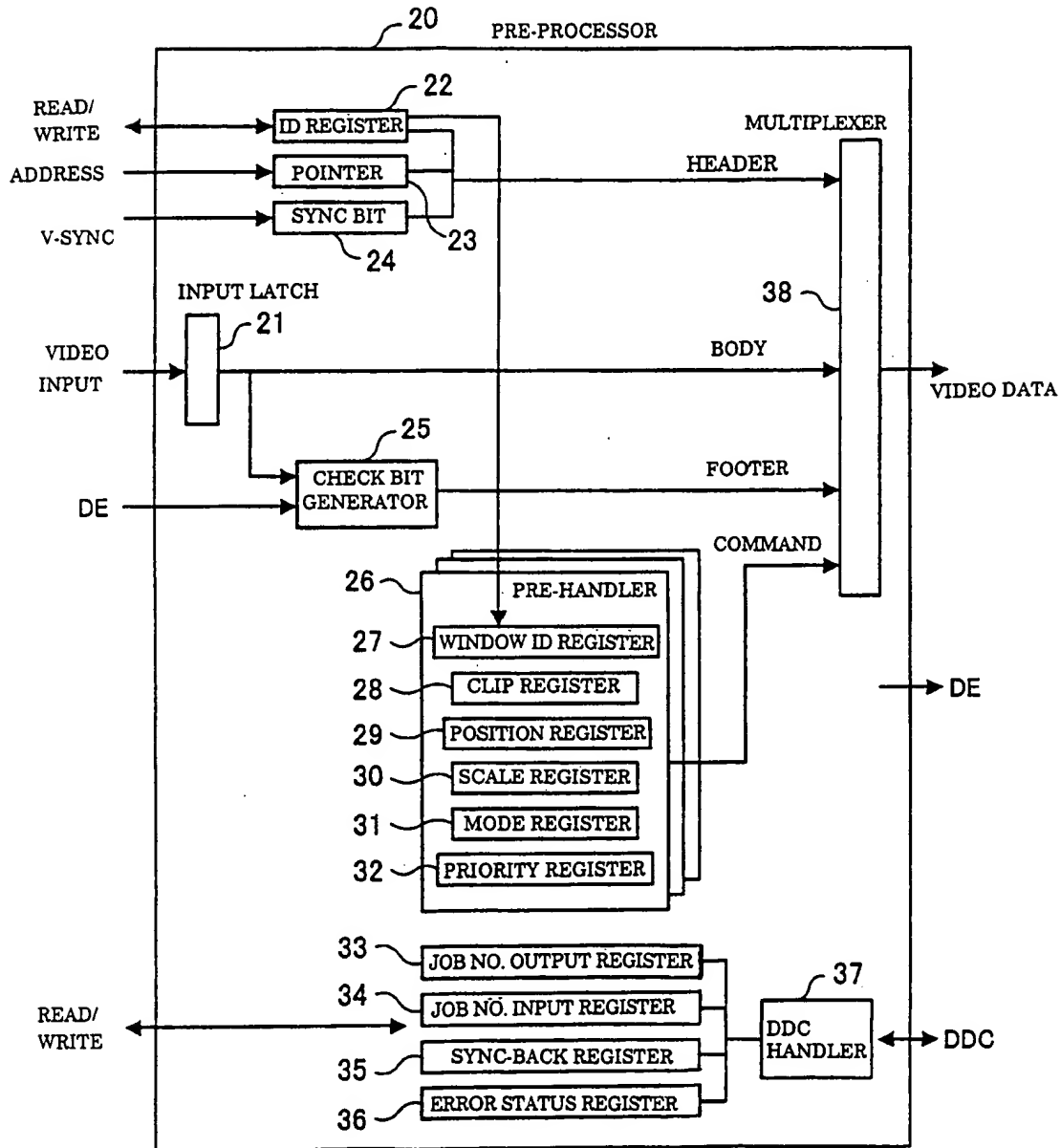
- The **DIGITAL I/F LINE** (49) connects to a component (53) and a component (69).
- Component (53) is connected to a **PANEL CONTROL CHIP** (51) via a component (68).
- Component (69) is connected to a **PANEL CONTROL CHIP** (51) via a component (70).
- Each **PANEL CONTROL CHIP** (51) is connected to **PANEL MEMORY** (52).
- The **PANEL CONTROL CHIPS** (51) are connected to a large **PANEL** (54) via a bus (55).
- The **PANEL** (54) is also connected to the **PANEL CONTROL CHIPS** (51) via a bus (54).

```

graph LR
    subgraph 11 [11]
        16[DAC] --- 20[PRE-PROCESSOR]
        17[ADDRESS GENERATOR] -- ADDRESS --> 20
        17 -- DE --> 20
    end
    20 -- VIDEO OUTPUT --> 15[INTERFACE TRANSCEIVER]
    20 -- DE --> 15
    15 -- DATA OUTPUT --> DO[DATA OUTPUT]
    15 <--> DDC[DDC]

```

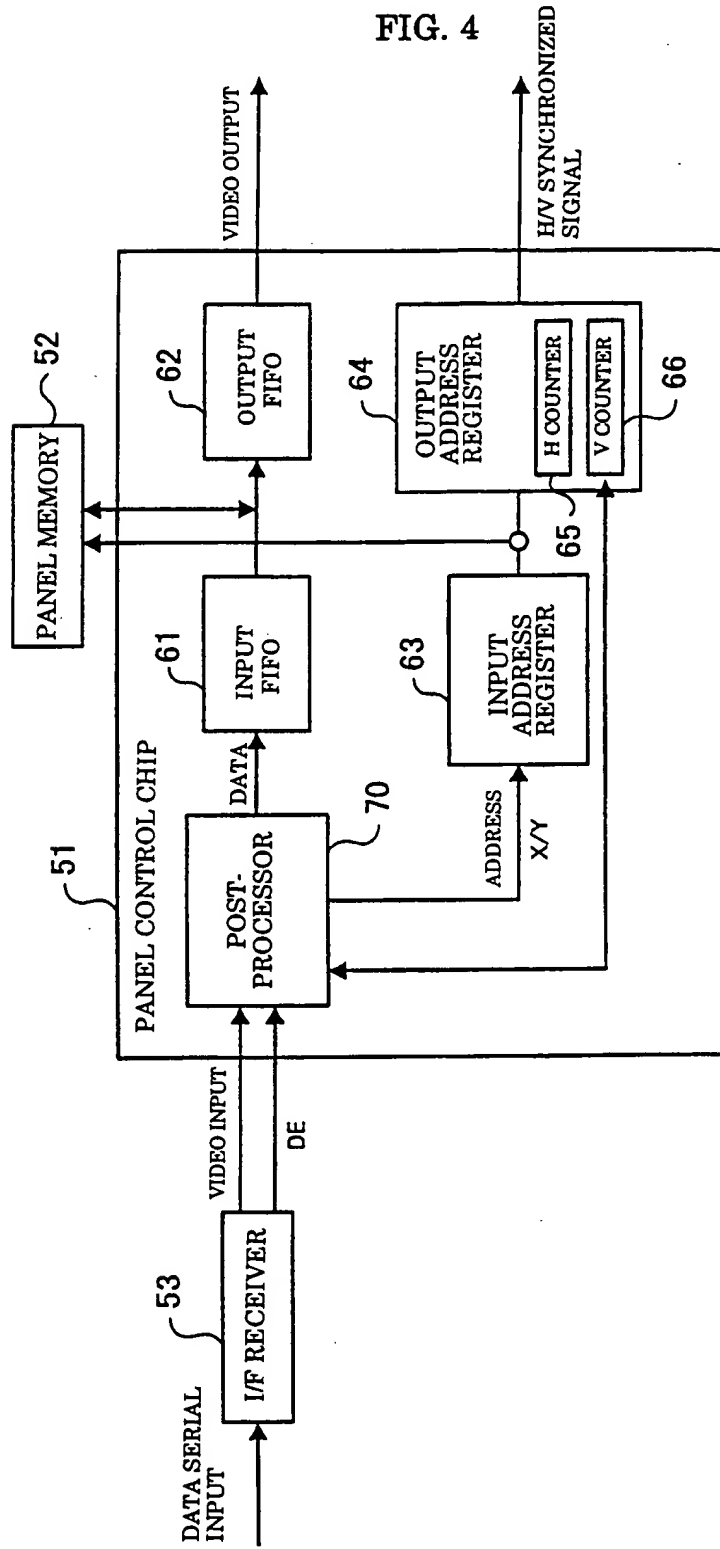
FIG. 3



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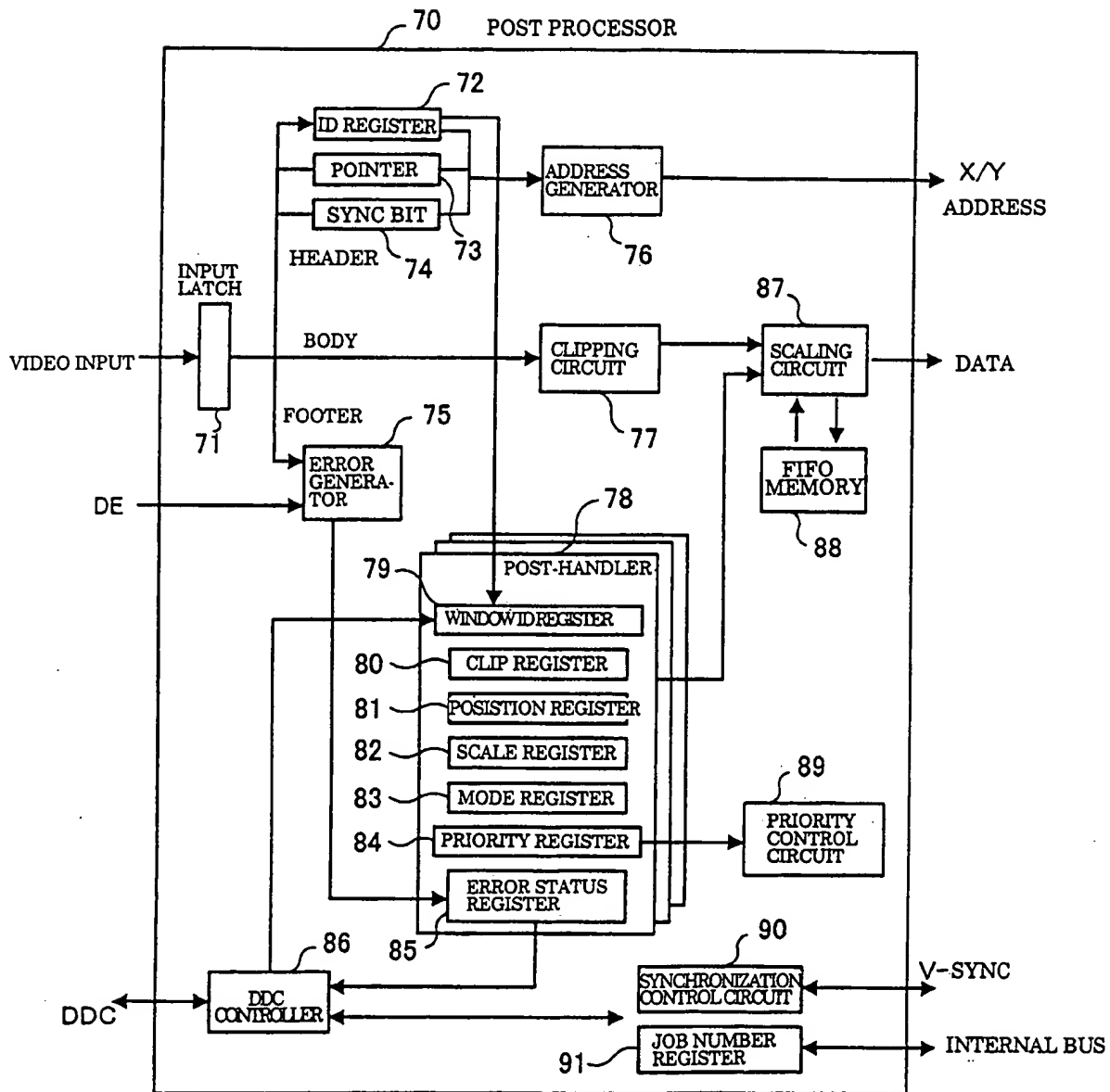
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FIG. 4



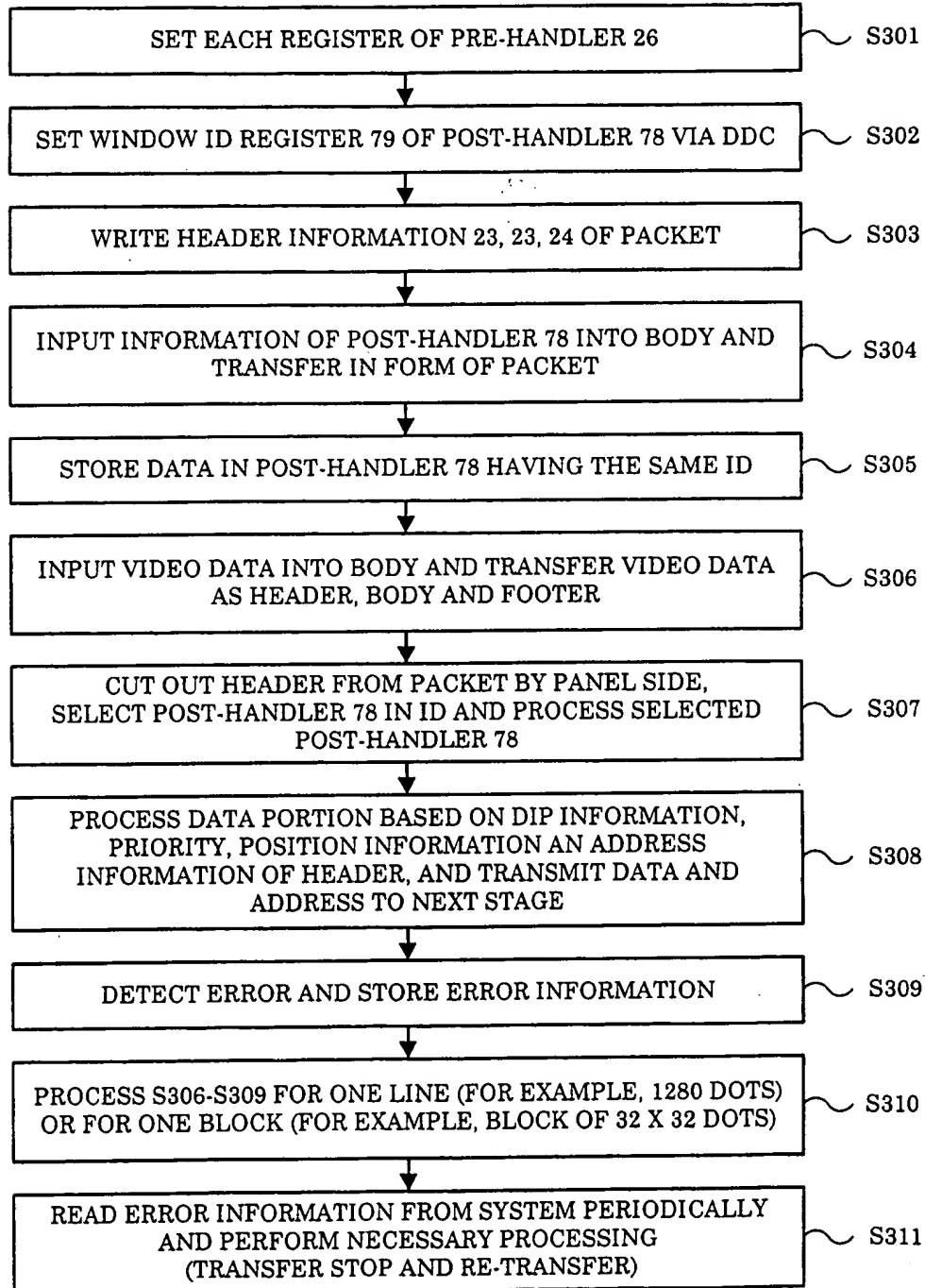
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FIG. 5



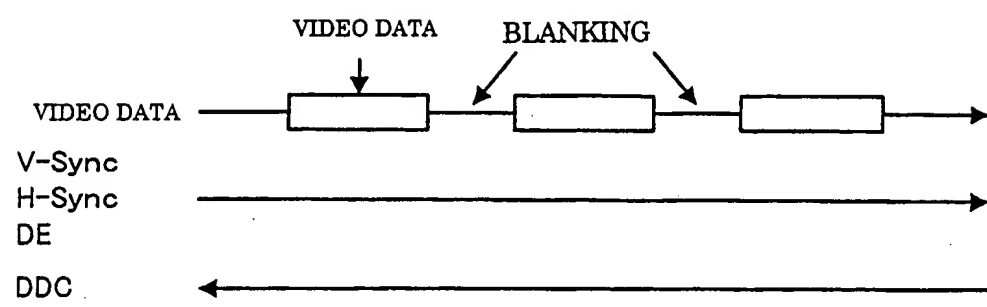
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FIG. 6

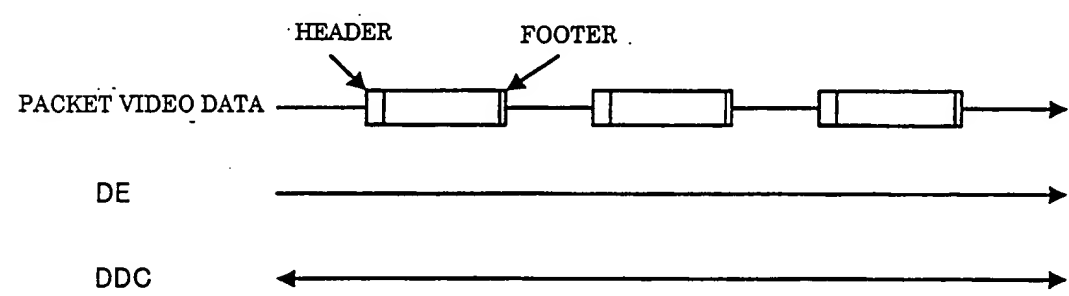


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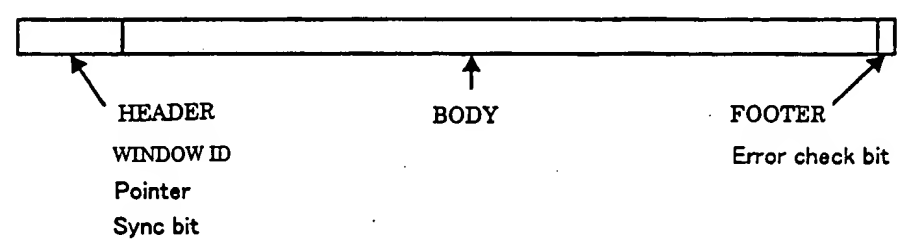
FIG. 7



(a) CONVENTIONAL TRANSFER OF VIDEO DATA



(b) TRANSFER OF VIDEO DATA IN THIS EMBODIMENT



(c) FORMAT OF PACKET VIDEO DATA

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FIG. 8

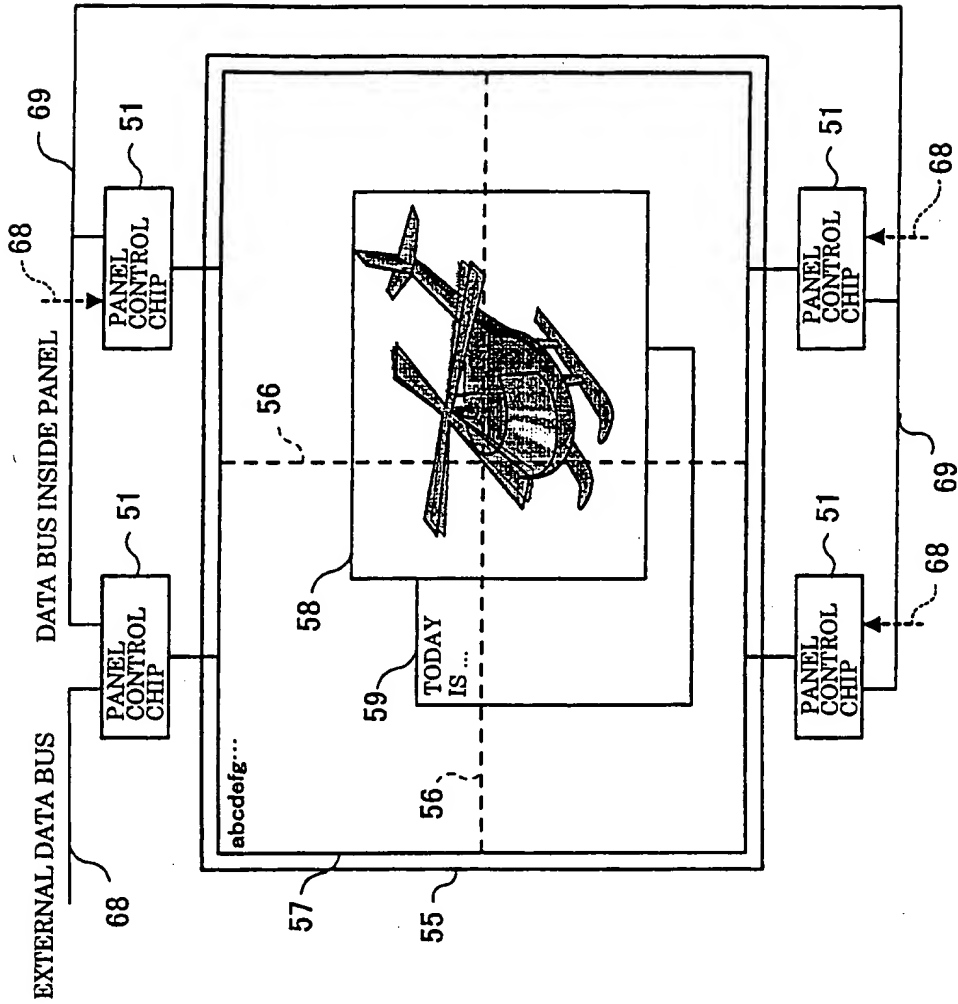
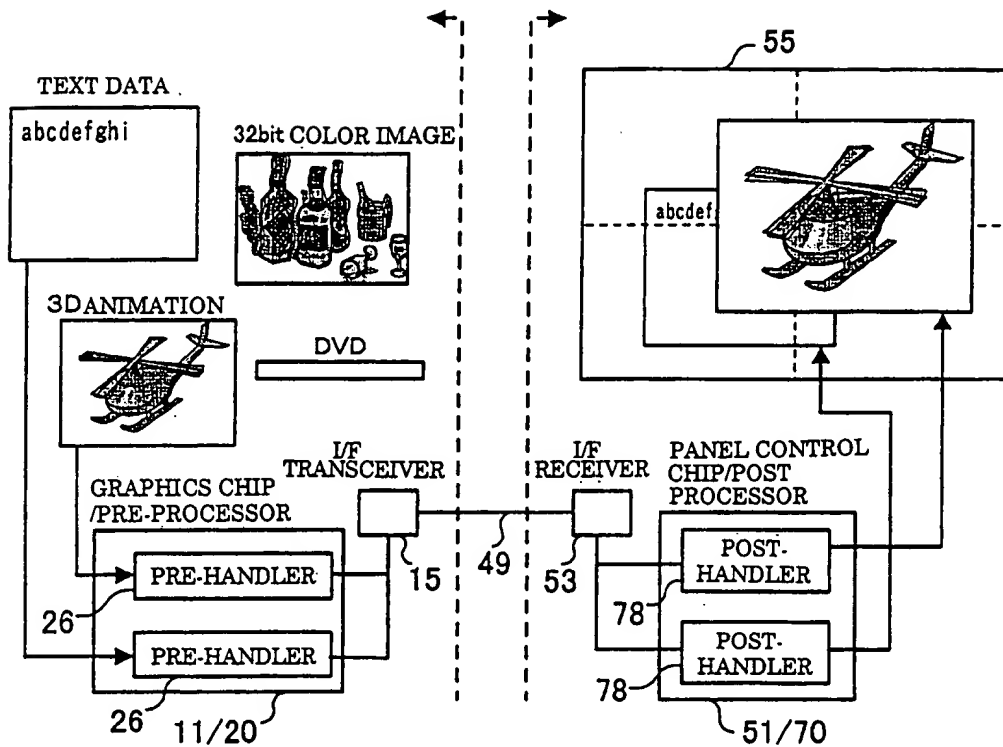
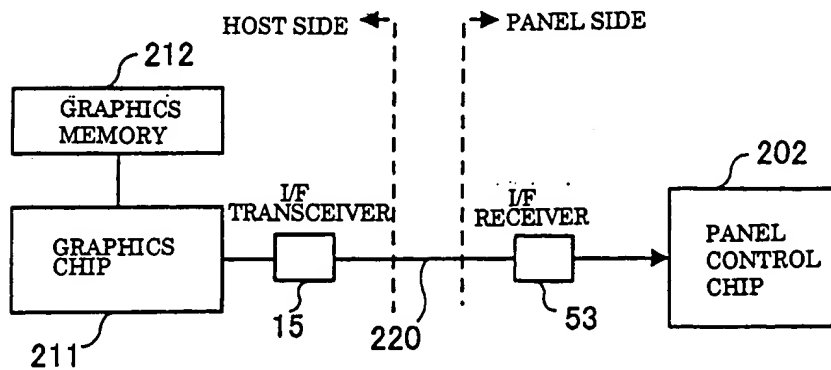




FIG. 9



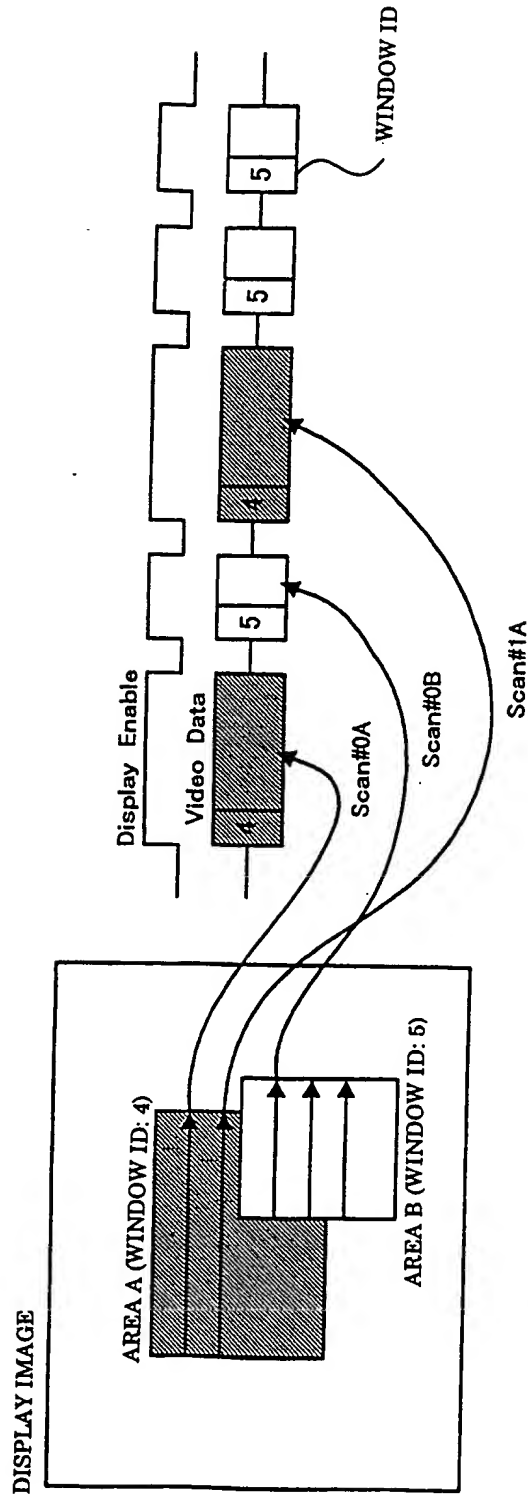
(a) DATA SOURCE AND PROCESSING SYSTEM



(b) LIMITATION OF DATA BAND WIDTH

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FIG. 10



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[illegible]

The diagram illustrates a system architecture divided into two main sections: **HOST SIDE 10** and **PANEL SIDE 50**, connected by a **DDC** (Data Display Channel) line.

**HOST SIDE 10:** This section contains the **GRAPHICS CHIP/PRE-PROCESSOR** (11/20). It includes a **SYNCHRONIZATION CONTROL CIRCUIT** (43) with an **OFFSET REGISTER** (41), an **ADDER** (42), a **MULTIPLEXER** (44), and a **VERTICAL SYNCHRONIZATION COUNTER** (45). The **H-Sync** signal is input to the adder. The output of the multiplexer is connected to the **DDC HANDLER** (37) on the panel side. The **DDC HANDLER** (37) is also connected to the **DDC** line and the **READ/WRITE CONTROL** (45). The **READ/WRITE CONTROL** (45) is connected to the **to CPU** line. The **DDC HANDLER** (37) is connected to the **JOB NO. OUTPUT REGISTER** (33) and the **JOB NO. INPUT REGISTER** (34). The **JOB NO. OUTPUT REGISTER** (33) is connected to the **DDC** line.

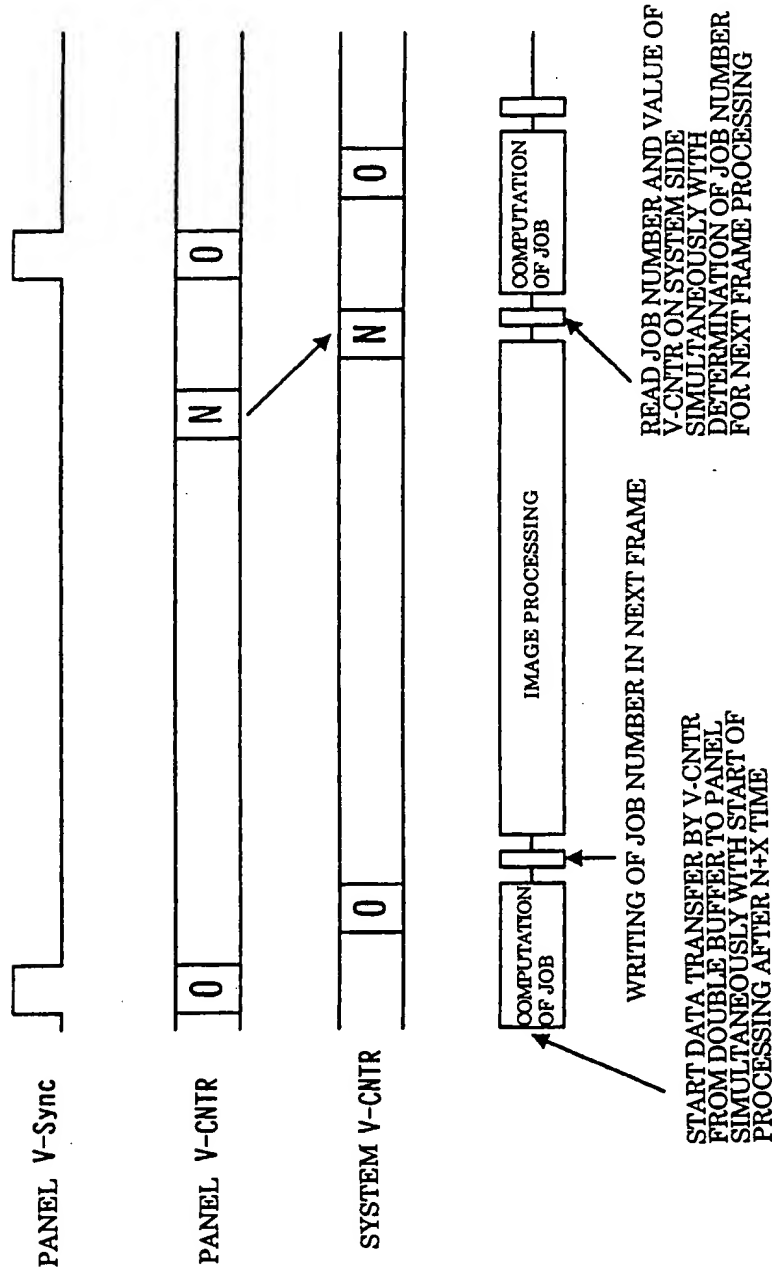
**PANEL SIDE 50:** This section contains the **PANEL CONTROL CHIP/POST PROCESSOR** (51/70). It includes a **SYNCHRONIZATION CONTROL CIRCUIT** (113) with an **OFFSET REGISTER** (113), an **ADDER** (114), and a **VERTICAL SYNCHRONIZATION COUNTER** (111). The **INT\_HSYNC** and **INT\_VSYNC** signals are inputs. The output of the adder is connected to the **DDC HANDLER** (115) on the host side. The **DDC HANDLER** (115) is also connected to the **DDC** line and the **COMP. RATOR** (119). The **COMP. RATOR** (119) is connected to the **JOB NO. OUTPUT REGISTER** (118) and the **JOB NO. INPUT REGISTER** (117). The **JOB NO. OUTPUT REGISTER** (118) is connected to the **DDC** line. The **JOB NO. INPUT REGISTER** (117) is connected to the **INTERNAL BUS CONTROLLER** (120). The **INTERNAL BUS CONTROLLER** (120) is connected to the **INT\_BUS** (121).



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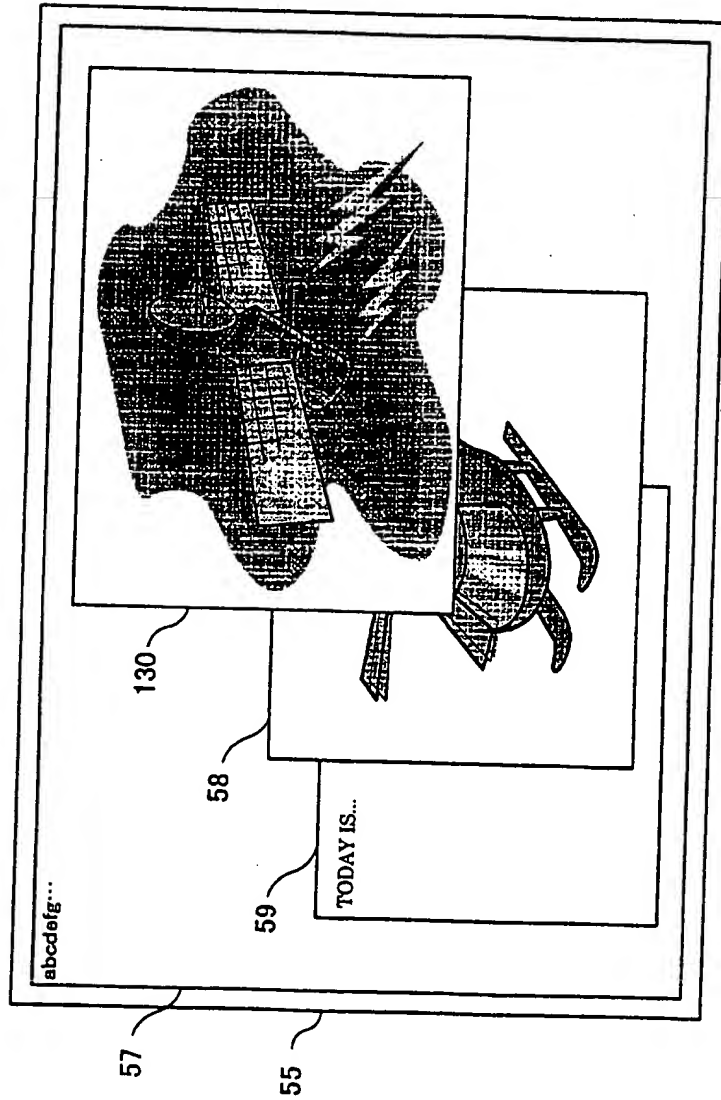
FIG. 14



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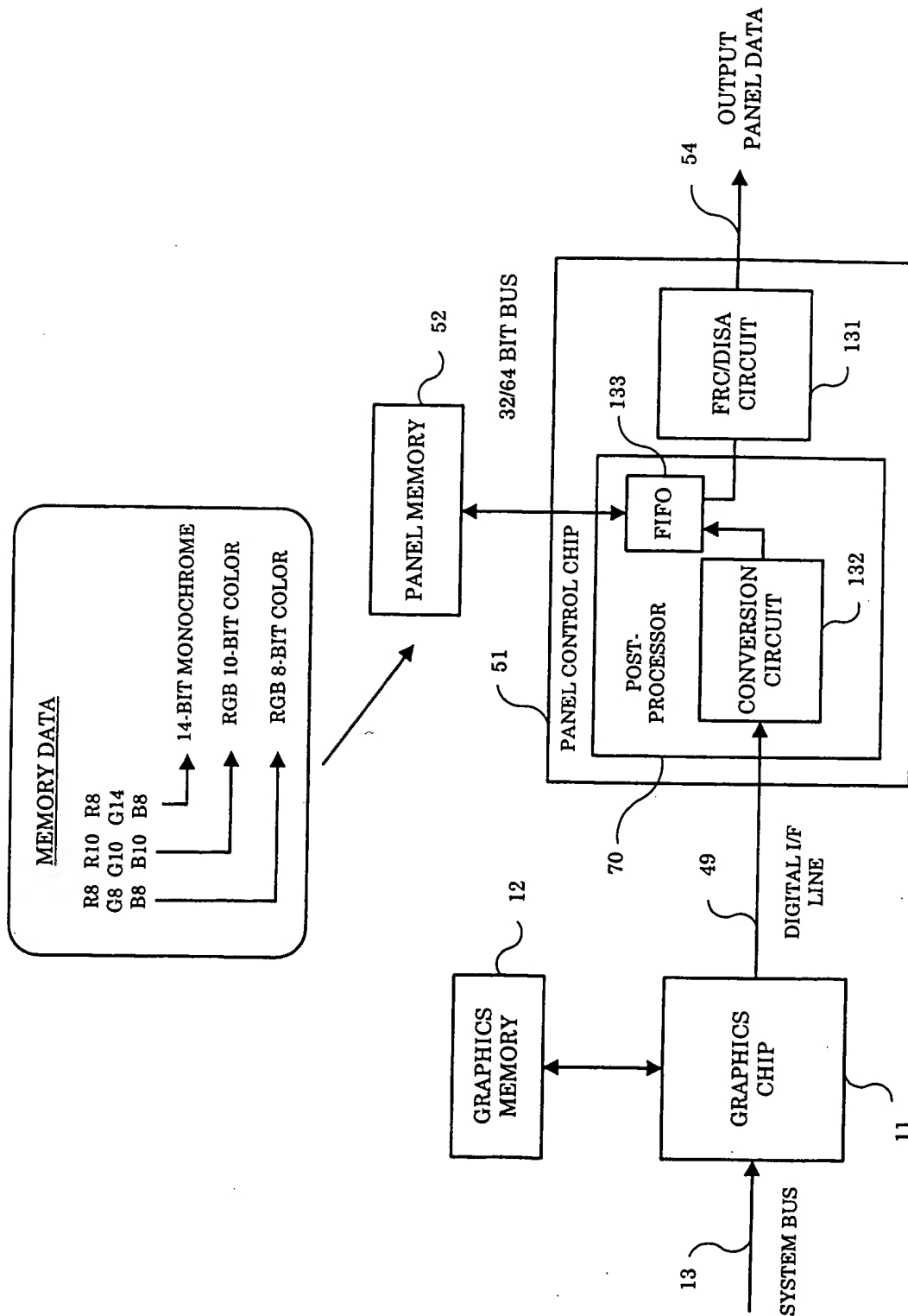
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FIG. 15



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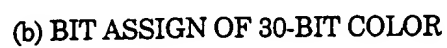
FIG. 16





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FIG. 18

